REMARKS

The Examiner is thanked for the thorough review and consideration of the present application. The non-final Office Action dated May 15, 2003 has been received and its contents carefully reviewed.

By this Response, Applicant has amended claims 1, 5 and 32. Claims 1-46 are currently pending, with claims 14-31 being withdrawn from consideration as being drawn to a non-elected species. No new matter has been added. Reconsideration and withdrawal of the rejections in view of the above amendments and the following remarks are requested.

In the Office Action , claims 1-13 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. Applicant has amended claim 1 to correct the typographical error and correctly recite the protrusion extends from the common line 114 as depicted in enlarged portion "D" of FIG. 3. Reconsideration and withdrawal of the rejection of claims 1-13 are requested.

In the Office Action, claims 32-46 are rejected under 35 U.S.C. § 103(a) as being unpatentable over alleged Admitted Prior Art in view of U.S. Patent No. 5,182,620, issued to Shimada et al. (hereafter "Shimada"). As a preliminary matter, Applicant makes no admission as to prior art. Figures 1 and 2A-2D, which are referenced by the Examiner, are used by the Applicant to provide Related Art descriptions. Applicant respectfully traverses the rejection because the Related Art and Shimada, analyzed alone or in any combination, fail to teach or suggest the combined features recited in the claims of the present application. In particular, the Related Art and Shimada fail to teach or suggest a liquid crystal display device that includes, among other features, "a protrusion extending from the common line and having a portion located under a corner of said common electrodes", as recited in amended claim 32. Since the Related Art and Shimada fail to teach or suggest at least this feature of claim 32, independent claim 32 and its dependent claims 33-46 are patentable over the Related Art and Shimada. Reconsideration and withdrawal of the rejection are requested.

Claims 32-37 and 40-44 are rejected under 35 U.S.C. § 103(a) as being unpatentable over the Related Art in view of U.S. Patent No. 6,424,397, issued to Kuo. Applicant respectfully

traverses the rejection because Kuo is not valid prior art against the claims of the present application. Applicant has a priority date of May 10, 2000, based upon Korean Application No. 2000-24965, which antedates the June 2, 2000 filing date of Kuo. Applicant files herewith a certified English translation of Korean Application No. 2000-24965 to perfect priority. As such, Applicant requests withdrawal of the rejection.

Claims 32-37 and 40-44 are rejected under 35 U.S.C. § 103(a) as being unpatentable over the Related Art in view of U.S. Patent No. 6,509,939, issued to Lee et al. (hereafter "Lee") or its foreign equivalent KR 2000007760A. Applicant traverses the rejection because neither the Related Art nor Lee, analyzed alone or in combination, teach or suggest a liquid crystal display device that includes, among other features, "a protrusion extending from the common line and having a portion located under a corner of said common electrodes", as recited in amended claim 32. Applicant respectfully notes that the Examiner incorrectly equated the common electrode 7 in Lee to the protrusion 116 recited in the claims of the present application. As such, the Related Art and Lee fail to provide a device having the combined features recited in independent claim 32, and claim 32 and its dependent claims 33-36 are patentable over the Related Art and Lee. Reconsideration and withdrawal of the rejection of claims 32-37 and 40-44 are requested.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

If the Examiner deems that a telephone conversation would further the prosecution of this application, the Examiner is invited to call the undersigned at (202) 496-7500.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed

Dated: August 14, 2003

Respectfully submitted,

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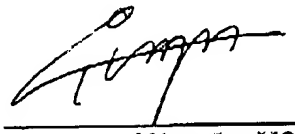
VERIFICATION OF TRANSLATION

I, Chan-Joo YOUN of 901 Seoyoung Bldg., 158-12, Samsung-dong, Kangnam-ku, Seoul, 135-090, Korea, declare that I have a thorough knowledge of the Korean and English languages, and the writings contained in the following pages are correct English translation of the specification and claims of Korean Patent Application No. 2000-24965.

This 12th day of August, 2003

By: 

[Chan-Joo YOUN]

KOREAN INDUSTRIAL

PROPERTY OFFICE

This is to certify that the following application annexed hereto

is a true copy from the records of the Korean Industrial Property Office

Application Number : **2000 year Patent Application 24965, PATENT-2000-0024965**

Date of Application : **May 10, 2000**

Applicant(s) : **LG. Philips LCD Co., Ltd.**

COMMISSIONER

[BIBLIOGRPHICAL DOCUMENTS]

[TITLE OF DOCUMENT] PATENT APPLICATION

[CLSSIFICATION] PATENT

[RECIPIENT] COMMISSIONER

[SUBMISSION DATE] 05. 10. 2000

[TITLE OF INVENTION IN KOREAN] 횡전계방식 액정표시장치용 어레이기판 제조방법

[TITLE OF INVENTION IN ENGLISH] METHOD FOR FABRICATING ARRAY SUBSTRATE FOR IN PLANE SWITCHING MODE LIQUID CRYSTAL DISPLAY DEVICE

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[ALL-INCLUSIVE AUTHORIZATION REGISTRATION NUMBER] 1999-001832-7

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[PURPORT] We submit application as above under the article 42 of the Patent Law.

Attorney Jung, Won-Ki (seal)

[FEES]

[BASIC APPLICATION FEE]	20 pages	29,000	won
[ADDITIONAL APPLICATION FEE]	3 pages	3,000	won
[PRIORITY FEE]	0 things	0	won
[EXAMINATION REQUEST FEE]	0 clamis	0	Won
[TOTAL]		32,000	Won

[ENCLOSED] 1. Abstract, Specifications (with Drawings) - 1 set

[DOCUMENT OF ABSTRACT]

[ABSTRACT]

The present invention relates to a liquid crystal display device, and more particularly, to a method of fabricating an array substrate for an in plane switching mode LCD device in which a common electrode and a pixel electrode are formed on the same substrate and drive liquid crystal molecules.

When fabricating the array substrate for an IPS mode LCD device, the residues of a metallic material, which remains in step portions of a common line parallel to a gate line, can cause a short-circuit between a data line and a storage capacitor. In order to prevent the short-circuit, a protrusion of a quadrilateral ring shape extended from a first layer of the double-layered common line is formed at both sides of the storage capacitor over the gate line. By forming an etching hole at each corner of the protrusion and completely eliminating the residues using the etching hole, the short-circuit between the storage capacitor and the data line is obviated. Accordingly, the IPS mode LCD device having a high resolution is achieved.

[REPRESENTATIVE FIGURE]

FIG. 3

[SPECIFICATIONS]

[NAME OF INVENTION]

METHOD FOR FABRICATING ARRAY SUBSTRATE FOR IN PLANE SWITCHING MODE LIQUID CRYSTAL DISPLAY DEVICE

[BRIEF EXPLANATION OF FIGURES]

FIG. 1 is a plan view of an array substrate for a conventional in-plane switching mode liquid crystal display (IPS-LCD) device;

FIGS. 2A to 2D are cross-sectional views, which are taken alone lines II-II and III-III of FIG. 1, showing fabricating processes of an array substrate;

FIG. 3 is a plan view of an array substrate for an in-plane switching mode liquid crystal display (IPS-LCD) device according to an embodiment of the present invention; and

FIGS. 4A to 4D are cross-sectional views, which are taken alone lines IV-IV and V-V of FIG. 3, showing fabricating processes of an array substrate according to an embodiment of the present invention.

* Explanation of major parts in the figures *

111: substrate	112: quadrilateral ring pattern
113: double-layered gate line	113a: first gate layer
113b: second gate layer	114: double-layered common line
114a: first common line	114b: second common line
115: data line	116: etching hole

[DETAILED DESCRIPTION OF INVENTION]

[OBJECT OF INVENTION]

[TECHNICAL FIELD OF THE INVENTION AND PRIOR ART OF THE FIELD]

The present invention relates to a liquid crystal display (LCD) device, and more particularly, to a fabricating method of an array substrate for an in-plane switching mode liquid crystal display device (IPS-LCD).

In general, liquid crystal display device (LCD) includes a display panel which has upper and lower substrates attaching each other with interposed liquid crystals. Further, the display panel includes retardation films and polarizers on its exterior surfaces of the upper and lower substrates. As the LCD device is selectively comprised of the above-mentioned elements, it converts the state of incident light and changes light refractive index in order to have great brightness and high contrast ratio.

Although twisted nematic liquid crystals are usually used as a liquid crystal layer in a liquid crystal cell, the twisted nematic liquid crystals have limitations of being employed in the large-sized display panel because of unstable transmittance depending on viewing angles. Moreover, since the light transmittance varies depending on vertical viewing angle and is asymmetrically distributed compared to symmetric distribution in horizontal viewing angle, a range of reverse-image occurs when the viewing angel is vertically slanted. Thus, the viewing angle becomes narrow.

An in-plane switching (IPS) mode liquid crystal display (LCD) devices typically include a lower substrate where a pixel electrode and a common electrode are disposed, an upper substrate having no electrode, and a liquid crystal interposed between the upper and

lower substrates. The liquid crystal layer is driven by an electric field generated between the common electrode and the pixel electrode. The contrast ratio, gray inversion and viewing angle characteristic such as color-shift are improved due to this typical structure.

FIG. 1 is a plan view of an array substrate for a conventional in-plane switching (IPS) mode liquid crystal display (LCD) device. As shown, a gate line 14 and a common line 12 are formed on a substrate (see reference element 11 of FIG. 2A). The gate line 14 and the common line are parallel to and spaced apart from each other. A data lines 13 crossing the gate line 14 and the common line 12. A thin film transistor (TFT) "T" as a switching element is formed near the cross of the gate line 14 and the data line 13. (Since FIG. 1 shows only one pixel region, a lower common line of the gate line and an upper gate line of the common line are omitted.)

The gate line 14 and the common line 12 have a double-layered structure, respectively, in order to prevent signal delay of these lines.

Namely, a first layer is usually made of a substance having low electrical resistance, such as Aluminum (Al). However, Aluminum has such a problem that it is low in hardness and chemical resistance. So the open-circuit and oxidation easily occur during an etching process.

To overcome this problem, a second layer is formed on the first layer and is usually a substance having high hardness and good chemical resistance, such as Molybdenum (Mo) or Chromium (Cr).

The TFT "T" includes an active channel 15, a source electrode 17, a drain electrode 19 and a gate electrode 21.

In the above-mentioned structure, the data line 13 crosses the common line 12 and the gate line 14 to define a pixel region "P." A common electrode 23 and a pixel electrode

25 are formed in the pixel region "P."

A vertical pattern of the common electrode 23 vertically extends to the pixel region "P" when the second layer of the common line 12 is patterned.

The pixel electrode 25 is formed of a transparent conductive metal and a vertical pattern of the pixel electrode 25 is formed to correspond to the vertical pattern of the common electrode 23 with an insulating layer interposed therebetween. An upper horizontal pattern 25a connecting the vertical pattern of the pixel electrode 25 overlaps a portion of the common line 12 to form a storage capacitor "C."

During a patterning process of the data line 13, metallic materials for the data line 13 are not completely etched and remain at a step portion "A" of the common line 12.

These residual metallic materials exist in a dielectric layer of the storage capacitor "C" such that the short-circuit occurs between the data line 13 and the storage capacitor "C".

For more detail illustration, fabrication cross-sectional views will be shown.

As shown in FIG. 2A, a first gate line 14a (of FIG. 1) and a first gate electrode 21a is formed on a transparent substrate 11 by depositing and patterning a conductive metal having low electrical resistance, such as Aluminum (Al). The first gate electrode 21a extends from the first gate line 14a (of FIG. 1) along a direction.

Simultaneously, a first common line 12a is formed to be parallel to the first gate line.

Thereafter, a second gate line 14b (of FIG. 1), a second gate electrode 21b and a second common line 12b are formed on the substrate 11 by depositing and patterning the conductive metal having the high chemical resistance, such as Mo. Namely, the second gate line 14b (of FIG. 1) is formed on the first gate line 14a (of FIG. 1), the second gate electrode 21b is formed on the first gate electrode 21a, and the second common line 12b is formed on the first common line 12a, thereby a double-layered gate line 14, a double-layered gate

electrode 21 and a double-layered common line 12 completed.

Simultaneously, a common electrode 23 including a plurality of vertical patterns is formed. The plurality of vertical patterns vertically extend to a pixel region "P" (of FIG. 1) and are combined with a horizontal pattern 23a (of FIG. 1).

As shown in FIG. 2B, a gate insulation layer 27 (a first insulation layer) is formed on an entire surface of the substrate 11 by depositing or coating one of an inorganic substance including silicon nitride (SiNx) and silicon oxide (SiO2) and an organic substance including BCB (benzocyclobutene) and acrylic resin.

Subsequently, as shown in FIG. 2B, an active layer 15 and a ohmic contact layer 16 are formed on the gate insulation layer 27 by forming and patterning a semiconductor layer using an amorphous silicon or impurity(n type or p type)-doped amorphous silicon.

As shown in FIG. 2C, a data line 13 (of FIG. 1), a source electrode 17 and a drain electrode 19 are formed on the ohmic contact layer 16 by depositing and patterning a conductive metal such as tungsten (W), chromium (Cr) and molybdenum (Mo). The data line 13 (of FIG. 1) crosses the common line 12 and the gate line 14 (of FIG. 1) and source electrode 17 extends from the data line 13. The source and drain electrodes 17 and 19 are spaced apart from each other.

A portion of the ohmic contact layer 16 between the source and drain electrodes 17 and 19 is eliminated to form a channel region of the active layer 15.

At this time, the metals for the source and drain electrodes 17 and 19 remain at a step portion "A" of the common line 12 disposed in the pixel region "P" (of FIG. 1). The residual metals 31 extend to the data line 13 (FIG. 1).

A passivation layer 33 (a second insulation layer) is then formed on an entire surface of the substrate 11 by depositing an organic or inorganic insulating material. After that, a

drain contact hole 35 exposing a portion of the drain electrode 19 is formed by patterning the passivation layer 33.

Now, as shown in FIG. 2D, a pixel electrode 25 is formed on the passivation layer 33 having the drain contact hole 35 by depositing and patterning one of transparent conductive material such as indium tin oxide (ITO) and indium zinc oxide (IZO). One end of the pixel electrode 25 contacts the drain electrode 19 through the drain contact hole 35 and the other end of the pixel electrode 25 overlaps the common line 12 to constitute a storage capacitor "C."

A plurality of vertical patterns of the pixel electrode 25 is disposed in the pixel region "P" (of FIG. 1) to correspond the plurality of vertical patterns of the common electrode.

An array substrate for a conventional IPS mode LCD device is obtained through the above-mentioned processes.

According to aforementioned structure of the array substrate for an IPS mode LCD device, the residual metallic substances due to the step portions "A" of the common line 14 both sides of the storage capacitor may extend from the data line to the storage capacitor.

Thus, the residual metallic substances cause the short between the data line 13 (of FIG. 1) and the storage capacitor "C."

The short results in discharge of charges stored in the storage capacitor "C" through the data line 13 (of FIG. 1). Moreover, the residual metallic substances may move to the pixel region to deteriorate the driving characteristics of the liquid crystals and bring about the point defect in the display panel.

[TECHNICAL SUBJECT OF INVENTION]

Therefore, to overcome the problems described above, the present invention provides

an array substrate for an IPS mode LCD device that prevents occurrence of a short-circuit between a data line and a storage capacitor due to residual metallic material at a step portion of a common line, and a fabricating method thereof.

[CONSTRUCTION AND OPERATION OF INVENTION]

To achieve these and other objects and in accordance with the purpose of the present invention, as embodied and broadly described, an array substrate for an IPS mode LCD device includes: a substrate; a double-layered gate line on a substrate, the double-layered gate lines including first and second gate layers that overlap each other; a double-layered common line parallel to the double-layered gate line, the double-layered common line including first and second common layers that overlap each other and being formed of the same layer and the same material as the double-layered gate line; a common electrode including a plurality of vertical patterns vertically extending from the second common layer; an insulation layer on the double-layered gate line; a plurality of data lines on the insulation layer, the plurality of data lines crossing the double-layered gate line and the common line; a pixel electrode including a plurality of vertical patterns corresponding to the plurality of vertical patterns of the common electrode and two horizontal patterns combining the plurality of vertical patterns, one horizontal pattern overlapping the double-layered common line to form a storage capacitor; a quadrilateral ring pattern extending from the first common layer at both sides of the storage capacitor; and a passivation layer on the pixel electrode, the passivation layer having an etching hole exposing a corner of the quadrilateral ring pattern adjacent to the data line.

In another aspect, a method of fabricating an array substrate for an IPS mode LCD device includes: providing a substrate; forming a double-layered gate line, a double-layered

common line, first and second quadrilateral ring patterns and a common electrode on a substrate, the double-layered common line being parallel to the double-layered gate line and including first and second common layers, the quadrilateral ring pattern extending from the first common layer and being disposed adjacent to a virtual line perpendicular to the gate line, the common line including a plurality of vertical patterns extending from the second common layer; forming an insulation layer on the double-layered gate line, the double-layered common line and the first and second quadrilateral ring patterns; forming a semiconductor layer of an island shape on a gate electrode, the semiconductor layer including an active layer and an ohmic contact layer; forming a data line, and source and drain electrodes on the semiconductor layer, the data line parallel to the virtual line and perpendicular to the double-layered gate line and the double-layered common line to define a pixel region, the source electrode extending from the data line to the active layer, the drain electrode being spaced apart from the source electrode; forming a drain contact hole and an etching hole by forming and patterning a passivation layer on the source and drain electrodes, the drain contact hole exposing the drain electrode and the etching hole exposing a corner of the quadrilateral ring pattern; forming a transparent metallic layer on the passivation layer by deposition; and forming a pixel electrode including a lower horizontal pattern, a vertical pattern and an upper horizontal pattern by patterning the transparent metallic layer, the lower horizontal pattern contacting the drain electrode through the drain contact hole, the vertical pattern vertically extending from the lower horizontal pattern and corresponding to the vertical pattern of the common electrode in the pixel region, the upper horizontal pattern combining the vertical pattern and overlapping the double-layered common line to constitute a storage capacitor, wherein a step of forming the pixel electrode includes a step of etching the gate insulation layer in the etching hole and a portion of the quadrilateral ring pattern under the gate

insulation layer.

In a method of fabricating an array substrate for an IPS mode LCD device, the first gate layer and the first common layer are made of one of a metallic material group having low resistance and including aluminum or aluminum alloy.

In a method of fabricating an array substrate for an IPS mode LCD device, the second gate layer and the second common layer are made of one of a conductive metallic material group having high chemical resistance and including molybdenum and tungsten.

Hereinafter, reference will now be made in detail to the preferred embodiment of the present invention, example of which is illustrated in the accompanying drawings.

In the present invention, a protrusion extends from a first common line at sides of a storage capacitor to a pixel region and an etching hole is formed in an upper edge of the protrusion. The present invention provides a method of removing residual metallic materials disposed from a data line to a storage capacitor along a protrusion by etching the protrusion through the etching hole.

FIG. 3 is a plan view of an array substrate for an in-plane switching (IPS) mode liquid crystal display (LCD) device according to an embodiment of the present invention.

As shown, a protrusion 112 of a quadrilateral ring shape is formed by extending a first common line 114a of double-layered common line 114 at both sides of a storage capacitor "C."

A second common line 114b is formed on the first common line 114a including the protrusion 112 of a quadrilateral ring shape. A vertical pattern of a common electrode extends from the second common line 114b to a pixel region.

The protrusion 112 does not overlap the second common line 114b and is protruded under the second common line 114b.

Since residual metallic materials 139a existing around interior step portions of the protrusions having a quadrilateral ring shape (the protrusion will be referred to as a quadrilateral ring pattern hereinafter) do not affect a short-circuit between the storage capacitor "C" and the data line 115, it is not necessary to remove the residual metallic materials. However, residual metallic materials 139b existing around exterior step portions of the quadrilateral ring pattern 112 can connect the data line 115 to the storage capacitor "C", and thus cause the short-circuit between the data line 115 and the storage capacitor "C".

To overcome this problem, therefore, an etching hole 116 is formed at an edge of the quadrilateral ring pattern 112 and the residual metallic materials around exterior step portions of the quadrilateral ring pattern 112 can be removed through the etching hole.

FIGS. 4A to 4D are cross-sectional views, which are taken alone lines IV-IV and V-V of FIG. 3, showing fabricating processes of an array substrate according to an embodiment of the present invention.

As shown in FIG. 4A, a first gate line 113a (of FIG. 3), a first gate electrode 117a and a first common line 114a are formed on a substrate 111 by depositing and patterning a conductive metallic material having low electrical resistance, such as Aluminum (Al). The first gate electrode 117a extends from the first gate line 113a (of FIG. 3) and the first common line 114a is parallel to the first gate line.

Simultaneously, a quadrilateral ring pattern 112 is formed to extend to a lower pixel region of the first common line 114a passing the pixel region "P" (of FIG. 3).

A plurality of (at least two) quadrilateral ring patterns 112 is formed in the pixel region "P."

Thereafter, a second gate line 113b (of FIG. 3), a second common line 114b and a second gate electrode 117b are formed on the first gate line 113a, the first common line 114b and the first gate electrode 117a, respectively, by depositing and patterning a conductive metallic material having high hardness and chemical resistance, such as Cr and Mo. Namely, the second gate line 113b (of FIG. 3) is formed to cover the first gate line 113a, the second common line 114b is formed to cover the first common line 114a, and the second gate electrode 117b is formed to cover the first gate electrode 117a. Thus, a double-layered gate line 113 (of FIG. 3), a double-layered common line 114 and a double-layered gate electrode 117 are completed.

Here, a common electrode 119 including a plurality of vertical patterns extending from the second common line 114b to the pixel region "P."

Here, the quadrilateral ring pattern 112 is formed not to overlap the second common line 114b overlapping the first common line 114a.

A gate insulation layer 131 (a first insulation layer) is formed on an entire surface of the substrate 111 having the double-layered common line 114, the common electrode 119 and the quadrilateral ring pattern 112 by depositing or coating one of an inorganic insulation material including silicon nitride (SiN_x) and silicon oxide (SiO_2) and an organic insulation material including benzocyclobutene (BCB) and acrylic resin.

As shown in FIG. 4B, an active layer 133 and an ohmic contact layer 134 are formed on the gate insulation layer 131 by subsequently depositing and patterning amorphous silicon and impurity-doped amorphous silicon.

As shown in FIG. 4C, a data line 115 (of FIG. 1), and source and drain electrodes 135 and 137 are formed on the ohmic contact layer 134 by depositing and patterning a conductive metallic material including tungsten (W), chromium (Cr) and molybdenum (Mo). The data

line 115 (of FIG. 1) crosses the gate line 113 (of FIG. 3). The source electrode 135 is extended from the data line 115 (of FIG. 1) over the double-layered gate electrode 117 and the drain electrode 137 is spaced apart from the source electrode 135.

At this time when forming the data line 115 and the source and drain electrodes 135 and 137, residual metallic materials 139a and 139b for the drain electrode 137 may be left around step portions of quadrilateral ring pattern 112. Since the residual metallic material 139a that is left around the interior step portion of the quadrilateral ring pattern 112 does not contact the data line 115 (of FIG. 1), it does not cause any defect in the array substrate. However, the residual material 139b that is left around the exterior step portion of the quadrilateral ring pattern 112 exists and disperses from the gate line 115 (of FIG. 1) to the storage capacitor that is formed in a later step. Thus, the residual material 139b results in short-circuit and point defect in the array substrate.

In order to remove the residual metallic material 139b that is left around the exterior step portion of the quadrilateral ring pattern 112, the particular method is required and that method is explained hereinafter.

A passivation layer (a second insulation layer) 141 is formed on and over the above-mentioned intermediates by depositing or coating one of organic and inorganic insulating materials. After that, a drain contact hole 139 that exposes a portion of the drain electrode 137 is formed by patterning the passivation layer 141. Simultaneously, an etching hole 116 is formed at an upper corner of the quadrilateral ring pattern 112.

Therefore, the residual metallic material 139b that is in the exterior step portion of the quadrilateral ring pattern 112 is eliminated by the dry etch during a process of forming the etching hole 116.

If the residual material 139b is not completely removed during that dry-etching

process, it can be taken off entirely in a subsequent pattering step of a pixel electrode.

As shown in FIG. 4D, a transparent conductive material such as indium tin oxide (ITO) or indium zinc oxide (IZO) is deposited on the passivation layer 141 having the drain contact hole 139 and the etching hole 116. The transparent conductive material is patterned to form a pixel electrode 145 including a lower horizontal pattern, a plurality of vertical patterns and an upper horizontal pattern 145a. The lower horizontal pattern contacts the drain electrode 137 through the drain contact hole 139. The plurality of vertical patterns extend from the lower horizontal pattern and is disposed at an upper portion of the pixel region "P" (of FIG. 3). The upper horizontal pattern 145a combines plurality of vertical patterns and overlaps the common line 114.

Even if the residual metallic material 139b is not completely removed by the above-mentioned dry etch, it is entirely removed during this wet-etching process. Namely, using the wet etch method that is used to form the pixel electrodes 145, some portion of the quadrilateral ring pattern 112 which is exposed by the etching hole 116 is removed, and thus the residual metallic material can be completely removed.

Here, the plurality of vertical patterns of the pixel electrode 145 in the pixel region "P" (of FIG. 3) is disposed to correspond to the vertical pattern of the common electrode.

As described herein before, in the embodiment of the present invention, the short-circuit occurring between the storage capacitor and the data line is prevented.

These processes and structure can be applied to an array substrate for the other mode LCD device.

[EFFECT OF INVENTION]

Therefore, since an array substrate for an IPS mode LCD device has a structure

where short-circuit between the storage capacitor and the data line is prevented, an IPS mode LCD device having no point defect can be obtained.

[RANGE OF CLAIMS]

[CLAIM 1]

An array substrate for an IPS mode LCD device, comprising:

a substrate;

a double-layered gate line on a substrate, the double-layered gate lines including first and second gate layers that overlap each other;

a double-layered common line parallel to the double-layered gate line, the double-layered common line including first and second common layers that overlap each other and being formed of the same layer and the same material as the double-layered gate line;

a common electrode including a plurality of vertical patterns vertically extending from the second common layer;

an insulation layer on the double-layered gate line;

a plurality of data lines on the insulation layer, the plurality of data lines crossing the double-layered gate line and the common line;

a pixel electrode including a plurality of vertical patterns corresponding to the plurality of vertical patterns of the common electrode and two horizontal patterns combining the plurality of vertical patterns, one horizontal pattern overlapping the double-layered common line to form a storage capacitor;

a quadrilateral ring pattern extending from the first common layer at both sides of the storage capacitor; and

a passivation layer on the pixel electrode, the passivation layer having an etching hole exposing a corner of the quadrilateral ring pattern adjacent to the data line.

[CLAIM 2]

A method of fabricating an array substrate for an IPS mode LCD device, comprising:

providing a substrate;

forming a double-layered gate line, a double-layered common line, first and second quadrilateral ring patterns and a common electrode on a substrate, the double-layered common line being parallel to the double-layered gate line and including first and second common layers, the quadrilateral ring pattern extending from the first common layer and being disposed adjacent to a virtual line perpendicular to the gate line, the common line including a plurality of vertical patterns extending from the second common layer;

forming an insulation layer on the double-layered gate line, the double-layered common line and the first and second quadrilateral ring patterns;

forming a semiconductor layer of an island shape on a gate electrode, the semiconductor layer including an active layer and an ohmic contact layer;

forming a data line, and source and drain electrodes on the semiconductor layer, the data line parallel to the virtual line and perpendicular to the double-layered gate line and the double-layered common line to define a pixel region, the source electrode extending from the data line to the active layer, the drain electrode being spaced apart from the source electrode;

forming a drain contact hole and an etching hole by forming and patterning a passivation layer on the source and drain electrodes, the drain contact hole exposing the drain electrode and the etching hole exposing a corner of the quadrilateral ring pattern;

forming a transparent metallic layer on the passivation layer by deposition; and

forming a pixel electrode including a lower horizontal pattern, a vertical pattern and an upper horizontal pattern by patterning the transparent metallic layer, the lower horizontal pattern contacting the drain electrode through the drain contact hole, the vertical pattern

vertically extending from the lower horizontal pattern and corresponding to the vertical pattern of the common electrode in the pixel region, the upper horizontal pattern combining the vertical pattern and overlapping the double-layered common line to constitute a storage capacitor,

wherein a step of forming the pixel electrode includes a step of etching the gate insulation layer in the etching hole and a portion of the quadrilateral ring pattern under the gate insulation layer.

[CLAIM 3]

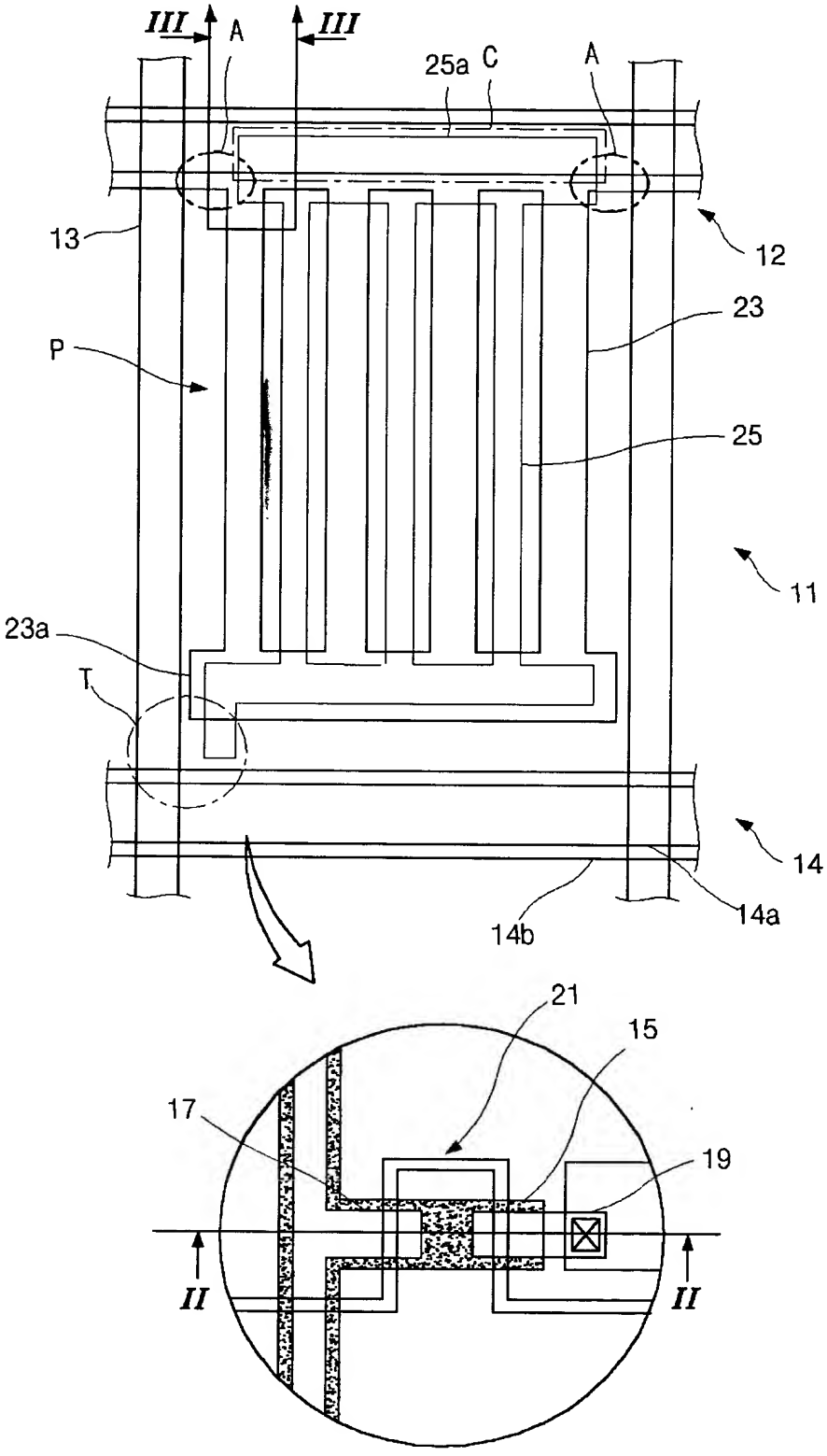
The method according to claim 2, wherein the first gate layer and the first common layer are made of one of a metallic material group having low resistance and including aluminum or aluminum alloy.

[CLAIM 4]

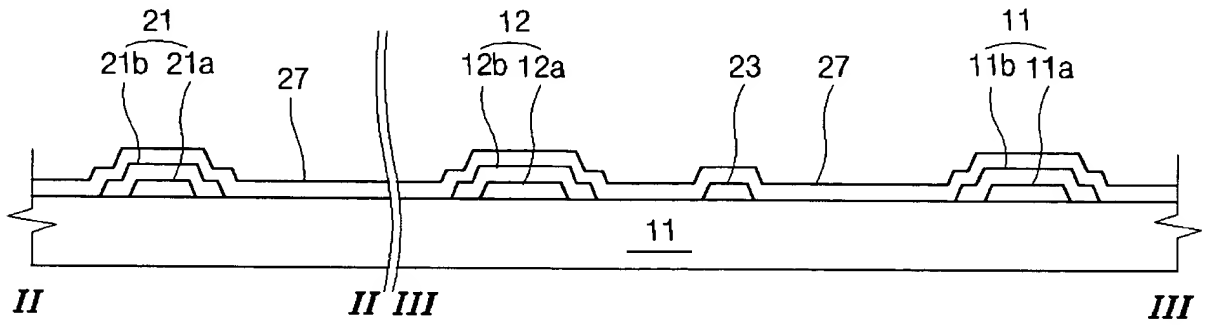
The method substrate according to claim 2, wherein the second gate layer and the second common layer are made of one of a conductive metallic material group having high chemical resistance and including molybdenum and tungsten.

[DRAWINGS]

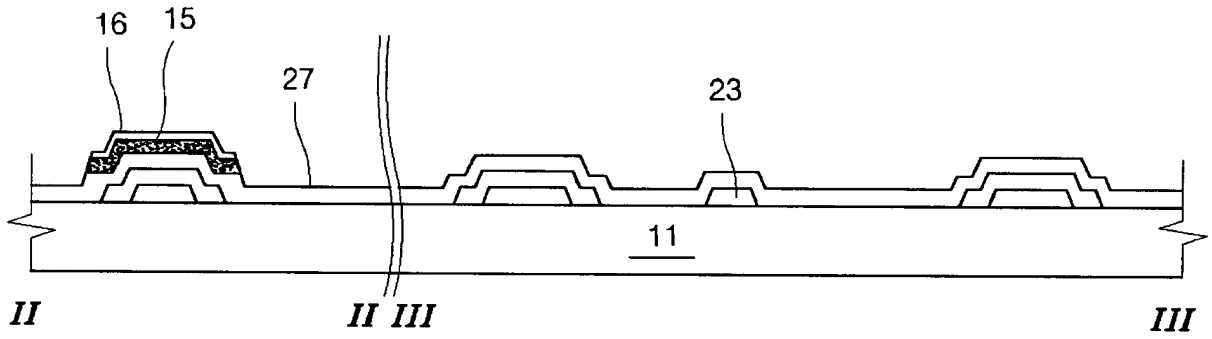
[Fig. 1]



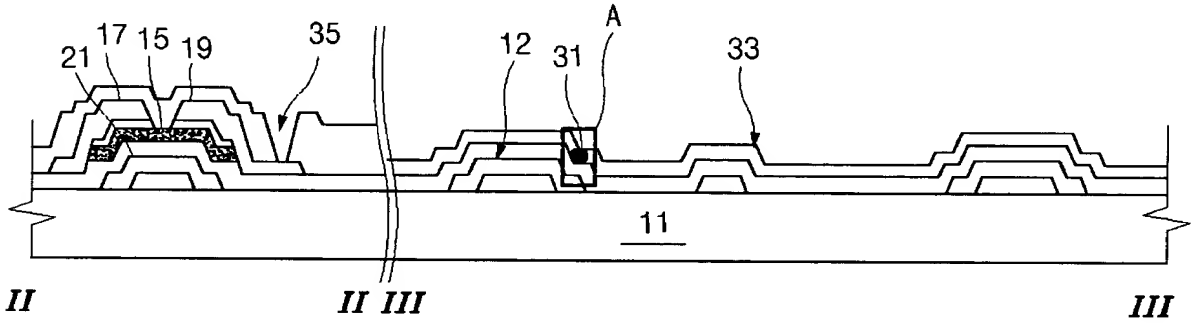
[Fig. 2a]



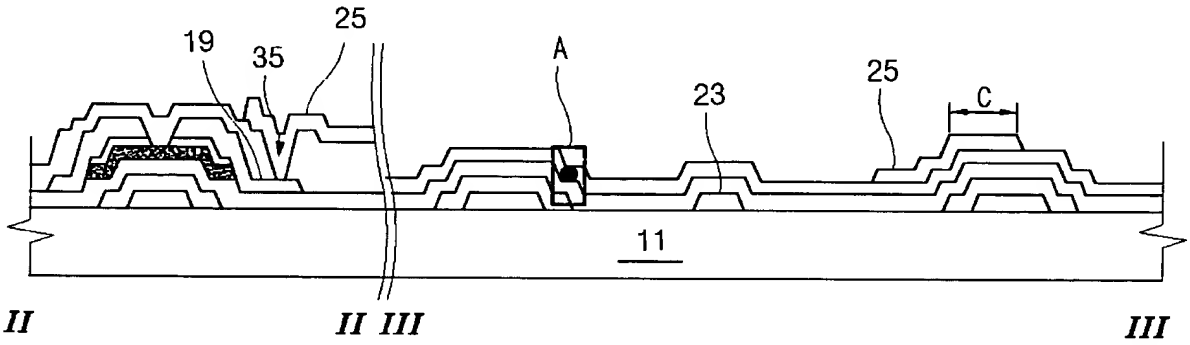
[Fig. 2b]



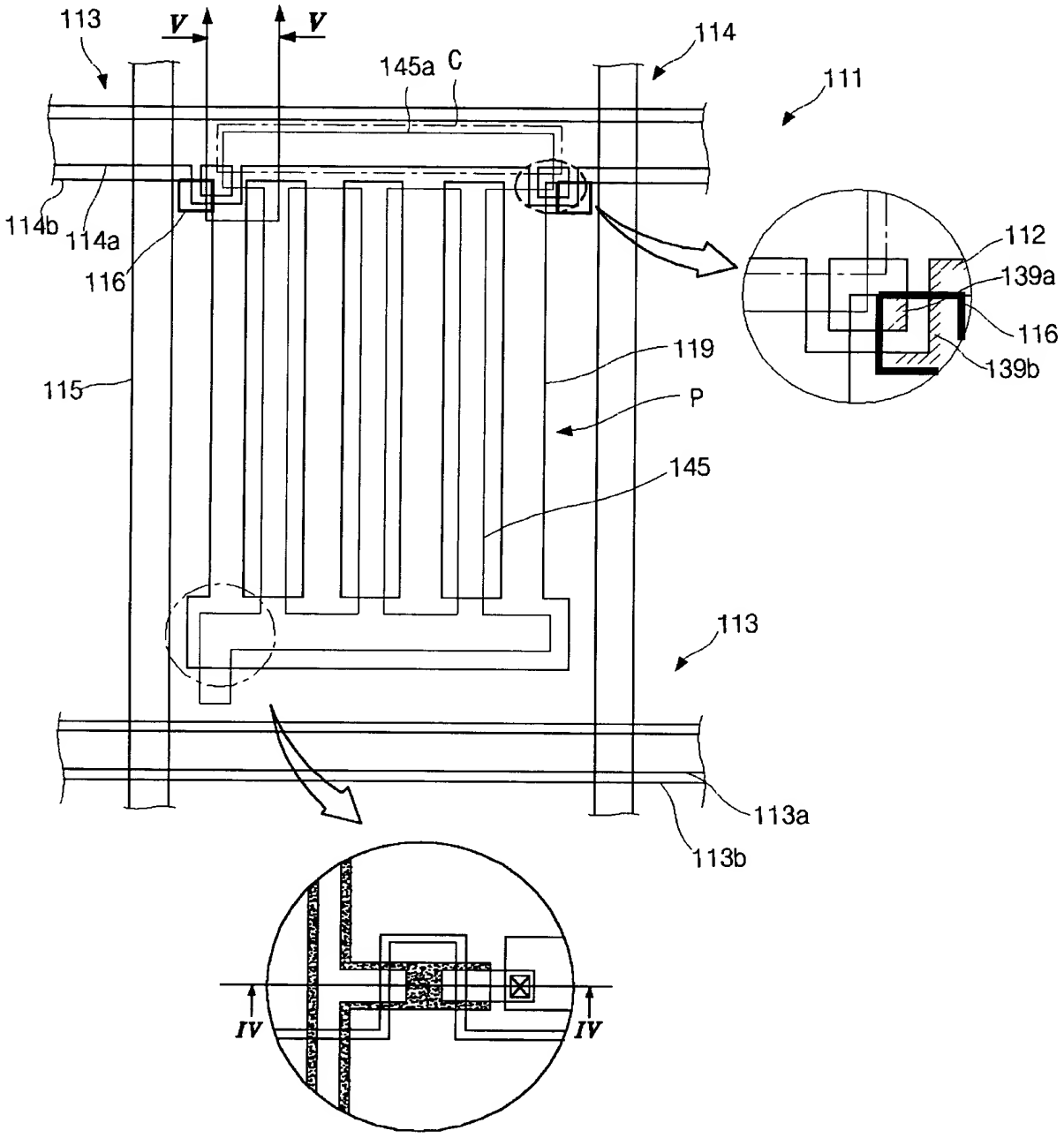
[Fig. 2c]



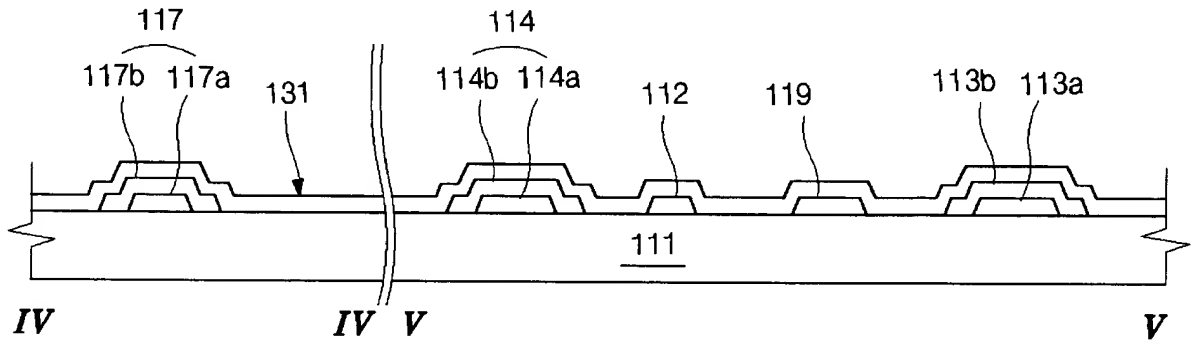
[Fig. 2d]



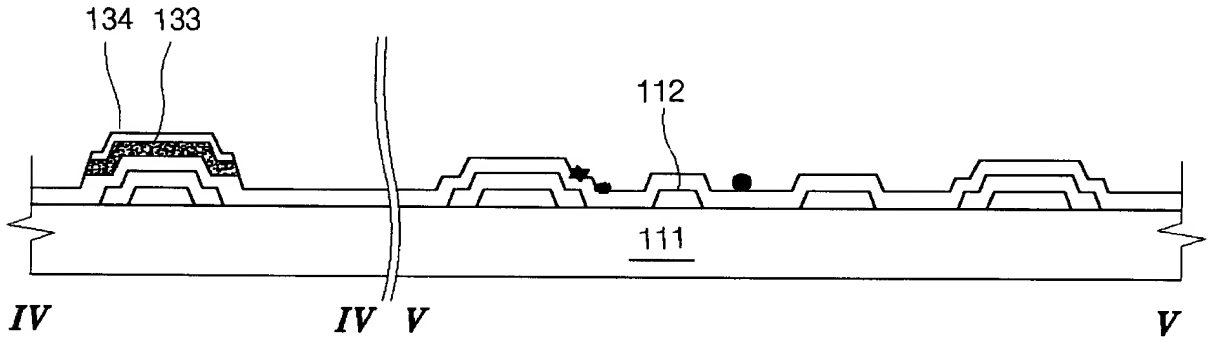
[Fig. 3]



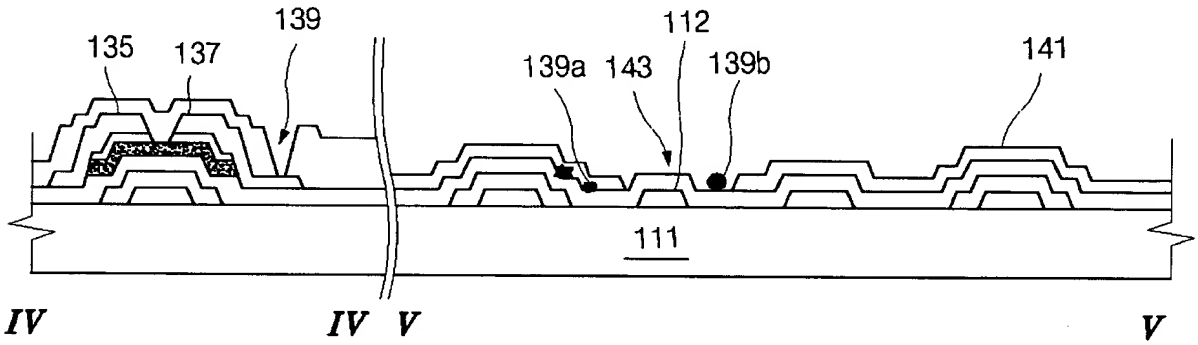
[Fig. 4a]



[Fig. 4b]



[Fig. 4c]



[Fig. 4d]